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In the Claims:

Please amend Claims 1-4 and 6 to read as follows:

A₁ 1. In a memory structure having a plurality of ordered memory levels, and forward and return paths for interconnecting said memory levels and a processor, each said memory level having a controller in said return path for receiving responses from an immediately higher one of said levels, if any, and for transmitting responses to an immediately lower one of said levels, except for the controller of the lowest one of said levels which transmits responses instead to said processor, each said controller having a buffer, a method of transferring requests from said processor on said forward path and responses to said requests on said return path to said processor, said method comprising the steps of:

transmitting each request from said processor to each of said levels;

if a request at any one of said levels is a read request addressed to the memory of said one level, then transmitting a response to said read request on said return path along with up to one other response from said buffer of said controller of said one level;

if a request at said any one of said levels is a write request addressed to the memory of said one level, then transmitting up to two responses from said buffer of said controller of said one level on said return path;

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if a request at said any one of said levels is addressed to one of said levels higher than said one level, then transmitting up to two responses from said buffer of said controller of said one level on said return path; and

if a request at said any one of said levels is addressed to one of said levels lower than said one level, then transmitting up to one response from said buffer of said controller of said one level on said return path.

A₁
2. A method as recited in claim 1, wherein at most three responses are stored in said buffer of said controller of any of said memory levels.

3. A memory structure for receiving requests to and transmitting responses from a memory in said structure, said structure comprising:

an ordered set of memory levels, each memory level having a controller and a memory unit, said memory unit being a portion of said memory;

a forward path for transmitting said requests to said memory levels; and

a return path for transmitting responses to said requests from any one of said levels which is higher than an immediately lower one of said levels to said immediately lower level;

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wherein said controller of said one level transmits responses to said requests on said return path to a buffer in said controller of said immediately lower level in accordance with the following algorithm:

- A₁
- a. if a request at said one level is a read request addressed to said one level, then transmitting a response to said read request on said return path, along with up to one response from said buffer of said controller of said one level, to said buffer of said controller of said immediately lower level,
 - b. if a request at said any one of said levels is a write request addressed to said one level, then transmitting no response to said write request on said return path and up to two responses from said buffer of said controller of said one level on said return path to said buffer of said controller of said immediately lower level,
 - c. if a request at said any one of said levels is addressed to one of said levels higher than said one level, then transmitting up to two responses from said buffer of said controller of said one level on said return path to said buffer of said controller of said immediately lower level, and
 - d. if a request at said any one of said levels is addressed to one of said levels lower than said one level, then transmitting up to one response from said buffer of said controller of said one level on said return path to said buffer of said controller of said immediately lower level.